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10/576,867	04/21/2006	Shunpei Yamazaki	740756-2953	9922

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NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
HANLEY, BRITT D	

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2889	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,867	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	BRITT D. HANLEY	2889	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

01 A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/21/2010 has been entered. Claims 1-25 are pending.

Claim Rejections - 35 USC § 103

02 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

03 The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

04 Claims 1, 2, 5, 6, 7, 10, 13, 14, 15, 18, 19, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki *et al.* (US 2001/0055841 A1) in view of Takao (JP 2003-058077 A) and Yamazaki *et al.* (US 6,355,941).

05 Hereinafter, Yamazaki *et al.* (US 2001/0055841 A1) is D1, Takao (JP 2003-058007 A) is D2, and Yamazaki et al. (US 6,355,941) is D3.

06 Regarding claims 1 and 14, D1 discloses a light emitting display device comprising: a a base film (302), gate electrode (304-307) formed over a base film (302); a gate insulating layer (372) formed over the gate electrode; a semiconductor layer (435) and a first electrode (383) formed over the gate insulating layer (Figure 4A); a wiring layer (382) formed over the semiconductor layer (Figure 4A); a partition wall (384) covering an edge portion of the first electrode and the wiring layer; an electroluminescent layer (385) over the first electrode (Figure 4A); and a second electrode (386) over the electroluminescent layer (Figure 4A). D1 does not explicitly appear to disclose (a) a base film including substance having a photocatalytic function between the substrate and gate electrode and the gate electrode formed over and in direct contact with the base film, or (b) the wiring layer covers the edge portion of the first electrode. The use of droplet discharge method is well known in the semiconductor art, and would have been obvious at the time of the invention to one of ordinary skill in the art.

07 However, in the same field of active-matrix devices, D2 discloses forming gate electrodes (26) on a substrate having a photocatalytic surface (TiO2) by ink jet method to simplify the manufacturing of a TFT array (¶ 12, 26-27). D2 does not disclose that the gate electrode is over and directly on the base film (see fig 10). However, it is well known in the art that TFT's can be arranged with the gate above the source/drain or below the source/drain. These configurations are functionally equivalent. Therefore, it would have been obvious to one of ordinary skill in the art to place the gate electrode below the drain/source electrodes and directly on the base layer. D2 teaches that the use of the photocatalytic base layer enables the creation of the source and drain electrodes directly on the base film by a ink jet method without the use of partitions (compare Figure 9 to Figure 10). The same benefit exists when forming the gate electrode directly on the base film.

08 Further, in the same field of active-matrix devices, D3 discloses a wiring layer (157) covering an edge portion (Figure 4A) of a first electrode (158) in order to connect to the first electrode (paragraph 119).

09 At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D3 to modify the device of D1 to include the photocatalytic surface of D2 in order to simplify TFT manufacturing and to cover an edge of the first electrode with the wiring as taught by D3 in order to connect the wiring to the electrode.

10 Regarding claims 2 and 15, the D1 discloses a light emitting display device comprising: base film (302); a wiring layer (382) and a first electrode (383) formed over a substrate (301) having an insulating surface; a semiconductor layer (435) formed over the wiring layer; a gate insulating layer (372) formed over the semiconductor layer; a gate electrode (339) formed over the gate insulating layer; a partition wall (384) covering an edge portion of the first electrode and the wiring layer; an electroluminescent layer (385) over the first electrode; and a second electrode (386) over the electroluminescent layer. D1 does not explicitly appear to disclose (a) a base film including a substance having a photocatalytic function and the wiring layer and the first electrode formed over and in direct contact with the base film, (b) the wiring layer covers the edge portion of the first electrode, or (c) the top gate TFT/ reverse staggered TFT configuration.

11 However, in the same field of active-matrix devices, D2 discloses forming wiring layers (22 & 23) over and in direct contact with a substrate having a photocatalytic surface (TiO2) by ink jet method to simplify the manufacturing of a TFT array (¶ 12, 26-27). It is well known in the art that TFT's can be arranged with the gate above the source/drain or below the source/drain. These configurations are functionally equivalent. Therefore, it would have been obvious to one of ordinary skill in the art to place the gate electrodes below the drain/source electrodes and directly on the base layer or vice-versa. D2 teaches that the use of the photocatalytic base layer enables the creation of the source and drain electrodes directly on the base film without the use of partitions (compare Figure 9 to Figure 10). The same benefit exist when forming the gate electrode directly on the base film.

12 Further, in the same field of active-matrix devices, D3 discloses a wiring layer (157) covering an edge portion (Figure 4A) of a first electrode (158) in order to connect to the first electrode (paragraph 119) and a reverse staggered TFT configuration (paragraphs 234-237, Figure 24).

13 At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D3 to modify the device of D1 to include the photocatalytic surface of D2 in order to simplify TFT manufacturing and to cover an edge of the first electrode with the wiring as taught by D3 in order to connect the wiring to the electrode. Further, the use of a reverse staggered TFT is a matter of design variation known in the art.

1.4 Regarding claims 4 and 17, the D1 discloses a light emitting display device comprising: a wiring layer (382) and a first electrode (383) formed over a substrate (301) having an insulating surface; a semiconductor layer (435) formed over the wiring layer; a gate insulating layer (372) formed over the semiconductor layer; a gate electrode (339) formed over the gate insulating layer; a partition wall (384) covering an edge portion of the first electrode and the wiring layer; an electroluminescent layer (385) over the first electrode; and a second electrode (386) over the electroluminescent layer, wherein the first electrode covers an edge portion of the wiring layer (Figure 4A). D1 does not explicitly appear to disclose (a) a base film including a substance having a photocatalytic function and the wiring layer and first electrode formed over and directly on the base film, or (b) the top gate TFT/ reverse staggered TFT configuration. The use of droplet discharge method is well known in the semiconductor art, and would have been obvious at the time of the invention to one of ordinary skill in the art.

1.5 However, in the same field of active-matrix devices, D2 discloses forming a wiring and first electrode (23 & 24) directly on a substrate having a photocatalytic surface (TiO2) by ink jet method to simplify the manufacturing of a TFT array (¶ 12, 26-27). It is well known in the art that TFT's can be arranged with the gate above the source/drain or below the source/drain. These configurations are functionally equivalent. Therefore, it would have been obvious to one of ordinary skill in the art to place the gate electrode below the drain/source electrodes and directly on the base layer. D2 teaches that the use of the photocatalytic base layer enables the creation of the source and drain electrodes directly on the base film without the use of partitions (compare Figure 9 to Figure 10). The same benefit exists when forming the gate electrode directly on the base film.

1.6 Further, in the same field of active-matrix devices, D3 discloses a reverse staggered TFT configuration (paragraphs 234-237, Figure 24).

1.7 At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D3 to modify the device of D1 to include the photocatalytic surface of D2 in order to simplify TFT manufacturing and the use of a reverse staggered TFT is a matter of design variation known in the art.

1.8 Regarding claims 5 and 18, the combination of D1-D3 disclose a light emitting display device according to any one of claims 1 to 2 or 14-15, wherein the substance having a photocatalytic function comprises titanium oxide (D2, paragraph 12). The motivation to combine is given above.

19 Regarding claims 6 and 19, D1 discloses a light emitting display device comprising: a substrate (301) having an insulating surface, a gate electrode (339) formed over the substrate; a gate insulating layer (372) formed over the gate electrode; a semiconductor layer (435) and a first electrode (383) formed over the gate insulating layer; a wiring layer (382) formed over the semiconductor layer; a partition wall (384) covering an edge portion of the first electrode and the wiring layer; an electroluminescent layer (385) over the first electrode; and a second electrode (386) over the electroluminescent layer. D1 does not appear to explicitly disclose (a) a conductive layer including a refractory metal over a substrate having an insulating surface and the gate electrode formed directly on the conductive layer, or (b) the wiring layer covers the edge portion of the first electrode. The use of droplet discharge method is well known in the semiconductor art, and would have been obvious at the time of the invention to one of ordinary skill in the art.

20 However, in the same field of active-matrix devices, D2 discloses forming gate electrodes on a substrate having a conductive layer including a refractory metal (Ti) by ink jet method to simplify the manufacturing of a TFT array (see at least paragraph 12). D2 does not disclose that the gate electrode is formed over and directly on the conductive layer(see fig 10). However, it is well known in the art that TFT's can be arranged with the gate above the source/drain or below the source/drain. These configurations are functionally equivalent. Therefore, it would have been obvious to one of ordinary skill in the art to place the gate electrode below the drain/source electrodes and directly on the conductive layer. D2 teaches that the use of the photocatalytic base layer enables the creation of the source and drain electrodes directly on the base film without the use of partitions (compare Figure 9 to Figure 10). The same benefit exists when forming the gate electrode directly on the conductive film.

21 Further, in the same field of active-matrix devices, D3 discloses a wiring layer (157) covering an edge portion (Figure 4A) of a first electrode (158) in order to connect to the first electrode (paragraph 119).

22 At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D3 to modify the device of D1 to include the conductive layer with a refractory metal of D2 in order to simplify TFT manufacturing and to cover an edge of the first electrode with the wiring as taught by D3 in order to connect the wiring to the electrode.

23 Regarding claims 7 and 20, D1 discloses a light emitting display device comprising: a substrate (301) having an insulating surface; a wiring layer (382) and a first electrode (383) formed over the substrate; a semiconductor layer (435) formed over the wiring layer; a gate insulating layer (372) formed over the semiconductor layer; a gate electrode (339) formed over the gate insulating layer; a partition wall (384) covering an edge portion of the first electrode and the wiring layer; an electroluminescent layer (385) over the first electrode; and a second electrode (386) over the electroluminescent layer. D1 does not explicitly appear to disclose (a) a substance conductive layer including a refractory metal over a substrate having an insulating surface, (b) the wiring layer covers the edge portion of the first electrode and both wiring layer and first electrode are formed over and in direct contact with the conductive layer, or (c) the top gate TFT/ reverse staggered TFT configuration. The use of droplet discharge method is well known in the semiconductor art, and would have been obvious at the time of the invention to one of ordinary skill in the art.

24 However, in the same field of active-matrix devices, D2 discloses forming wirings and first electrodes on a substrate having a conductive layer including a refractory metal (Ti) by ink jet method to simplify the manufacturing of a TFT array (see at least paragraph 12). D2 does not disclose that the wiring and first electrodes are formed over and directly on the conductive layer(see fig 10). However, it is well known in the art that TFT's can be arranged with the gate above the source/drain or below the source/drain. These configurations are functionally equivalent. Therefore, it would have been obvious to one of ordinary skill in the art to place the gate electrode below the drain/source electrodes and directly on the conductive layer. D2 teaches that the use of the photocatalytic base layer enables the creation of the source and drain electrodes directly on the base film without the use of partitions (compare Figure 9 to Figure 10). The same benefit exists when forming the gate electrode directly on the conductive film.

25 Further, in the same field of active-matrix devices, D3 discloses a wiring layer (157) covering an edge portion (Figure 4A) of a first electrode (158) in order to connect to the first electrode (paragraph 119) and a reverse staggered TFT configuration (paragraphs 234-237, Figure 24).

26 At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D3 to modify the device of D1 to include the conductive layer with a refractory metal of D2 in order to simplify TFT manufacturing and to cover an edge of the first electrode with the wiring as taught by D3 in order to connect the wiring to the electrode. Further, the use of a reverse staggered TFT is a matter of design variation known in the art.

27 Regarding claims 9 and 22, D1 discloses a light emitting display device comprising: a substrate (301) having an insulating surface; a wiring layer (382) and a first electrode (383) formed over the substrate; a semiconductor layer (435) formed over the wiring layer; a gate insulating layer (372) formed over the semiconductor layer; a gate electrode (339) formed over the gate insulating layer; a partition wall (384) covering an edge portion of the first electrode and the wiring layer; an electroluminescent layer (385) over the first electrode; and a second electrode (386) over the electroluminescent layer, wherein the first electrode covers an edge portion of the wiring layer (Figure 4A). D1 does not explicitly appear to disclose (a) a substance conductive layer including a refractory metal over a substrate having an insulating surface, (b) the wiring layer covers the edge portion of the first electrode and both wiring layer and first electrode are formed over and in direct contact with the conductive layer, or (c) the top gate TFT/ reverse staggered TFT configuration. The use of droplet discharge method is well known in the semiconductor art, and would have been obvious at the time of the invention to one of ordinary skill in the art.

28 However, in the same field of active-matrix devices, D2 discloses forming wirings and first electrodes on a substrate having a conductive layer including a refractory metal (Ti) by ink jet method to simplify the manufacturing of a TFT array (see at least paragraph 12). D2 does not disclose that the wiring and first electrodes are formed over and directly on the conductive layer(see fig 10). However, it is well known in the art that TFT's can be arranged with the gate above the source/drain or below the source/drain. These configurations are functionally equivalent. Therefore, it would have been obvious to one of ordinary skill in the art to place the gate electrode below the drain/source electrodes and directly on the conductive layer. D2 teaches that the use of the photocatalytic base layer enables the creation of the source and drain electrodes directly on the base film without the use of partitions (compare Figure 9 to Figure 10). The same benefit exists when forming the gate electrode directly on the conductive film.

29 Further, in the same field of active-matrix devices, D3 a reverse staggered TFT configuration (paragraphs 234-237, Figure 24).

30 At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D3 to modify the device of D1 to include the conductive layer with a refractory metal of D2 in order to simplify TFT manufacturing and the use of a reverse staggered TFT is a matter of design variation known in the art.

31 Regarding claims 10 and 23, the combination of D1-D3 discloses a light emitting display device according to any one of claims 6-9 or 19-22 wherein the refractory metal is selected from the group consisting of Ti (titanium), W (tungsten), Cr (chromium), A1 (aluminum), Ta (tantalum), Ni (nickel), Zr (zirconium), Hf (hafnium), V (vanadium), Ir (iridium), Nb (niobium), Pd (lead), Pt (platinum), Mo (molybdenum), Co (cobalt), and Rh (rhodium) (D2, paragraph 12). The motivation to combine is given above.

32 Regarding claims 11 and 24, the combination of D1-D3 discloses a light emitting display device according to any one of claims 1-4, 6-9, 14-17, and 19-22, wherein the gate electrode and the wiring layer are made of a material selected from the group consisting of silver, gold, copper, and indium tin oxide (D3, Cu, paragraph 145). At the time the invention was made, it would have been obvious to a person having ordinary skill in the art to use a metal such as copper, gold, or ITO in order to reduce electrical resistance or form a transparent electrode. Further, these are all well known electrode materials in the art.

33 Regarding claim 13, the combination of D1-D3 disclose a TV set including a display screen having the light emitting display device according to any one of claims 1-2 and 6-7 (D1, Figure 18A).

34 Regarding claims 12 and 25, the combination of D1-D3 disclose the light emitting display device according to any one of claims 1-4 and 6-9, wherein the semiconductor layer is a semi-amorphous semiconductor containing hydrogen and halogen and having a crystal structure (column 8, lines 31-46, D3). At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D3 to modify the device of D1 and D2 to include the semiconductor layer comprising a semi-amorphous semiconductor containing hydrogen and halogen and having a crystal structure of D3 in order to improve TFT operation (column 8, D3).

35 Claims 3, 8, 16, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki *et al.* (US 2001/0055841 A1) in view of Takao (JP 2003-058077 A).

36 Regarding claims 3 and 16, D1 discloses a light emitting display device comprising: a base film (302); a gate electrode (339) formed over a substrate (301) having an insulating surface; a gate insulating layer (372) formed over the gate electrode; a semiconductor layer (435) and a first electrode (383) formed over the gate insulating layer (Figure 4A); a wiring layer (382) formed over the semiconductor layer (Figure 4A); a partition wall (384) covering an edge portion of the first electrode and the wiring layer; an electroluminescent layer (385) over the first electrode (Figure 4A); and a second electrode (386) over the electroluminescent layer (Figure 4A), wherein the first electrode covers an edge portion of the wiring layer (Figure 4A). D1 does not explicitly appear to disclose (a) a base film including a substance having a photocatalytic function formed on the substrate and (b) the gate electrode formed over and in direct contact with the base film. The use of droplet discharge method is well known in the semiconductor art, and would have been obvious at the time of the invention to one of ordinary skill in the art.

37 However, in the same field of active-matrix devices, D2 discloses forming gate electrodes (26) on a substrate having a photocatalytic surface (TiO_2) by ink jet method to simplify the manufacturing of a TFT array (¶ 12, 26-27). D2 does not disclose that the gate electrode is over and directly on the base film (see fig 10). However, it is well known in the art that TFT's can be arranged with the gate above the source/drain or below the source/drain. These configurations are functionally equivalent. Therefore, it would have been obvious to one of ordinary skill in the art to place the gate electrode below the drain/source electrodes and directly on the base layer. D2 teaches that the use of the photocatalytic base layer enables the creation of the source and drain electrodes directly on the base film without the use of partitions (compare Figure 9 to Figure 10). The same benefit exists when forming the gate electrode directly on the base film.

38 At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D2 to modify the device of D1 to include the photocatalytic surface of D2 in order to simplify TFT.

39 Regarding claims 8 and 21, D1 discloses a light emitting display device comprising: a substrate (301) having an insulating surface, a gate electrode (339) formed over the substrate; a gate insulating layer (372) formed over the gate electrode; a semiconductor layer (435) and a first electrode (383) formed over the gate insulating layer; a wiring layer (382) formed over the semiconductor layer; a partition wall (384) covering an edge portion of the first electrode and the wiring layer; an electroluminescent layer (385) over the first electrode; and a second electrode (386) over the electroluminescent layer, wherein the first electrode covers an edge portion of the wiring layer (Figure 4A). D1 does not appear to explicitly disclose (a) a conductive layer including a refractory metal over a substrate having an insulating surface, (b) or that the gate electrode is formed over and in direct contact with the conductive layer.

40 However, in the same field of active-matrix devices, D2 discloses forming gate electrodes on a substrate having a conductive layer including a refractory metal (Ti) by ink jet method to simplify the manufacturing of a TFT array (see at least paragraph 12). D2 does not disclose that the gate electrode is formed over and directly on the conductive layer(see fig 10). However, it is well known in the art that TFT's can be arranged with the gate above the source/drain or below the source/drain. These configurations are functionally equivalent. Therefore, it would have been obvious to one of ordinary skill in the art to place the gate electrode below the drain/source electrodes and directly on the conductive layer. D2 teaches that the use of the photocatalytic base layer enables the creation of the source and drain electrodes directly on the base film without the use of partitions (compare Figure 9 to Figure 10). The same benefit exists when forming the gate electrode directly on the conductive film.

41 At the time the invention was made, it would have been obvious to a person having ordinary skill in the art having the references of D1-D2 to modify the device of D1 to include the conductive layer with a refractory metal of D2 in order to simplify TFT manufacturing.

Response to Arguments

42 Applicant's arguments filed 04/23/2010 have been fully considered but they are not persuasive. Applicant argues the prior art of record does not teach or suggest the newly added amendments. Specifically, "over in direct contact with" for claims 1-4 and 14-17 and "in direct contact with" for claims 6-9 and 19-22.

4.3 Examiner disagrees. D2 discloses that the base film/conductive layer is formed on the substrate and a reverse/staggered TFT (gate electrode above the drain/source) is formed directly on the base film. It is a matter of engineering design choice to form the TFT with the gate electrode above or below the drain and source. Both designs are functionally equivalent. In the gate below the drain/source, the gate electrode would have been formed directly on the base film/conductive layer.

4.4 The benefit of using the base film/conductive layer is to fabricate the structures of the TFT without the use of partitions or masks, And thereby simplify the manufacturing process. In both traditional and reverse/staggered TFT designs, this benefit is achieved.

4.5 Applicant also indicated that new claims 57-68 are distinguishable over the prior art. Examiner notes that only claims 1-25 are pending in the application (total amount of claims is 72).

Conclusion

4.6 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Britt Hanley whose telephone number is (571) 270-3042. The examiner can normally be reached on Monday - Thursday, 6:30a-5:00p ET.

4.7 If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minh-Toan Ton can be reached on (571)272-2303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

4.8 Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see *http://pair-direct.uspto.gov*. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Britt Hanley/ Examiner, Art Unit 2889	/Toan Ton/ Supervisory Patent Examiner, Art Unit 2889